[h2] **What is Claimed is:**

[1 (c1)]

A method of forming n-well and p-well regions on a substrate, comprising the steps of:

forming a first mask structure having a given thickness on the substrate;

carrying out n-well implants into regions of the substrate exposed by the first mask structure;

substantially reducing said thickness of said first mask structure;

carrying out a first p-well implant through said first mask structure, so that a first implant region is formed below the n-well and a second implant region is formed below the first mask structure;

forming a second mask structure on the substrate having an image generally complementary to the first mask structure; and

carrying out p-well implants into regions of the substrate exposed by the second mask structure.

[2 (c2)]

The method as recited in claim 1, wherein said step of carrying out a first p-well implant through the first mask structure does not increase threshold voltages of transistors subsequently formed adjacent an interface between said n-well and said p-well.

[3 (c3)]

The method as recited in claim 2, wherein said step of carrying out a first p-well implant through the first mask structure does not produce significant scattering of implanted ions.

[4 (c4)]

The method as recited in claim 1, wherein said first masking structure comprises a first layer disposed on the substrate and a second layer disposed on the first layer, said second layer being thicker than said first layer.

[5 (c5)]

The method of claim 4, wherein prior to said step of carrying out n-well implants said second layer is imaged to expose said regions of the substrate.

[6 (c6)]

The method of claim 5, wherein during said step of carrying out n-well implants said first layer prevents damage to the substrate.

[7 (c7)]

The method of claim 5, wherein prior to said step of carrying out a first p-well implant portions of said first layer exposed by said second layer are removed, and then remaining portions of said second layer are removed.

[8 (c8)]

The method as recited in claim 4, wherein said second layer is at least six times thicker than said first layer.

[9 (c9)]

The method as recited in claim 4, wherein said first layer is selected from a group consisting of polysilicon, silicon oxide, and silicon nitride.

[10 (c10)]

The method as recited in claim 4, wherein said first layer is approximately 100-300 nm thick.

[11 (c11)]

The method as recited in claim 9, wherein said step of carrying out a first p-well implant through the first mask structure does not produce significant scatterings of implanted ions.

[12 (c12)]

The method as recited in claim 4, wherein said second layer comprises photoresist.

[13 (c13)]

The method as recited in claim 12, wherein said photoresist is approximately 1800-2500nm thick.

[14 (c14)]

The method as recited in claim 9, wherein said step of carrying out a first p-well implant through the first mask structure is carried out at an energy of approximately 550 kEv.

[15 (c15)]

The method as recited in claim 14, wherein said step of carrying out a first p-well implant through the first mask structure is carried out at a dose of approximately 2.5 x 10 e 14 per cm2.

[16 (c16)]

The method as recited in claim 10, wherein said first masking layer is comprised of a material selected from the group consisting of polysilicon, silicon nitride, and silicon oxide.

[17 (c17)]

The method as recited in claim 16, wherein said first masking layer is approximately 100-300A thick.

[18 (c19)] A method of forming abutting retrograde n-well and p-well regions on a substrate, comprising the steps of:

forming the retrograde n-well by implanting with a first dopant species; and

forming the retrograde p-well by first carrying out a deep implant with a second dopant species under conditions that substantially reduce scattering of said second dopant species into abutting regions of said retrograde n-well.

[19 (c20)]

A method of forming retrograde n-well and p-well regions on a substrate, comprising the steps of:

forming a first mask structure on the substrate comprised of a first thin layer on the substrate and a second thick layer on said thin layer;

removing portions of said second layer; defining an image in said second layer

carrying out n-well implants into regions of the substrate beneath said removed portions of said second layer;

removing portions of said first layer;

carrying out a first p-well implant through said first layer so that a first implant region is formed immediately below the n-well and a second implant region is formed below the first mask structure;

forming a second mask structure on the substrate having an image generally complementary to the first mask structure; and

carrying out p-well implants into regions of the substrate exposed by the second mask structure.

[20 (c21)]

A CMOS device having FETs with effective channel lengths less than or equal to approximately 0.11um formed in adjacent, retrograde nwells and pwells, wherein threshold voltages of FETs formed with approximately 1.5 um of an interface between said nwells and pwells are constant within approximately 10 mV.